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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,051	11/29/2001	Andreas Wichern	DE 000214	5503

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/998,051	Applicant(s) WICHERN ET AL.	
	Examiner Linh V Nguyen	Art Unit 2819	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's amendment received on 10/28/03. Claims 4 and 10 have been amended. Claims 1 – 20, are pending on this application.

2.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1- 5, 7 – 11, 13, 14 and 16, are rejected under 35 U.S.C. 102(e) as being anticipated by Tiller et al. U.S Patent No. 5,933,711.

Regarding to claims 1, and 4, Fig. 4 of Tiller et al. discloses an amplifier circuit comprising: first differential amplifier stage (Q1, Q2) having a first and a second output branch; second differential amplifier stage (Q11, Q3, Q4) that is coupled to the first output branch of the first differential amplifier stage (Collector of Q1), the second differential amplifier stage having a first output branch (see Q3) and at least a second output branch (See Q11) for controllably dividing a first current in the first output branch of the first differential amplifier stage into partial currents, the second output branch (Q11) having at least one sub-ranch that is connected to a current power supply terminal (36); a third differential amplifier (Q12, Q5, Q6) stage that is coupled to the

second output branch of the first differential amplifier stage (See Q2), the third differential amplifier stage having a first output branch (See Q6) and at least a second output branch (Q12) for controllably dividing a second current in the second output branch of the first differential amplifier stage into partial currents; a first load impedance (RC) coupled to one of the output branches of the second differential amplifier stage (Q3) for generating a first output voltage (Vout+) from the partial current flowing in said one of the first output branches of the second differential amplifier stage; and a second load impedance (RC) coupled to one of the output branches of the third differential amplifier stage (Q6) for generating a second output voltage (Vout-) from the partial current flowing in said one of the first output branches of the third differential amplifier stage; wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively (See terminal between RC, Q11 or Q12, and 36).

Regarding to claim 2, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the first load impedance (See terminal between RC, Q11), and in that said one of the second output branches of the third differential amplifier stage has two jointly controlled sub branches, a first sub-branch of which is coupled to the second load impedance (See terminal between RC, Q12).

Regarding to claim 3, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap (Vout+) on the first load

impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap (Vout-) on the second load impedance.

Regarding to claim 5, wherein the variable amplifier comprising at least two controllable amplifier arrangements (Fig. 4), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (Vgc) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals (Fig. 4, differential inputs and differential outputs)

Regarding to claim 7, wherein the first amplifier differential stage comprises a plurality of bipolar transistors (Fig. 4).

Regarding to claim 8, wherein the second amplifier differential stage comprises a plurality of bipolar transistors (Fig. 2).

Regarding to claim 9, wherein the first load impedance is an ohmic resistor (RC).

Regarding to claim 10, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches (Q11, RC), a first sub-branch (Q11, RC) of which is coupled to the first load impedance (RC), and in that said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches (Q12, RC), a first sub-branch (Q12, RC) of which is coupled to the second load impedance (RC).

Regarding to claim 11, Fig. 4 Tiller et al. disclose the arrangement for variable gain amplifier circuit comprising at least two controllable amplifier arrangements (Fig. 4), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (Vgc) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of common control signal (Fig. 4 differential amplifier).

Regarding to claim 13, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap (Vout +) on the first load (RC) impedance, and said one of the second output braches of the third differential amplifier stage is coupled to a tap (Vout-) on the second load impedance (RC).

Regarding to claim 14, the variable gain amplifier comprising at least two controllable amplifier arrangements (Fig. 4), wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals (Vgc) and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals (Fig. 4 differential amplifier).

Regarding to claim 16, wherein the first differential amplifier stage comprises a plurality of bipolar transistors (Fig. 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 – 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tiller et al as applied to claims 1 and 4 above, and further in view of Brunner U.S. patent No. 6,046, 640.

Regarding to claim 17, Tiller et al. as applied to claims 1 and 4 above disclose every aspect of applicant's claimed invention except for a second impedance load (R1) coupled to the first impedance load and to the second output branch, and connected to a current power supply terminal.

Fig. 6 (24) of Brunner disclose an amplifier circuit having a second impedance load (R1) coupled to the first impedance load (Rc) and to the second output branch (Q22), and connected to a current power supply terminal (Vcc).

Tiller et al. and Brunner are analogous because both relating differential amplifier circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to applied the load impedance structures of Brunner's amplifier to the load impedance Rc of Tiller et al.'s amplifier for the purpose of providing changes gain by manipulating a loading network (Col. 3 lines 26 – 28).

7. Claims 6, 12 and 15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tiller et al as applied to claims 1 and 4 above, and further in view of Ishihara U.S patent No. 6,177,839.

Tiller et al. as applied to claims 1, 4, 5, 11 and 14 above disclose every aspect of applicant's claimed invention except for wherein the output branches of the second and the third differential amplifier stage are formed with transistor whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at different values of the common control signals in the individual controllable amplifier arrangements.

Fig. 1 of Ishihara discloses a variable gain amplifier having first and second and third differential amplifier stages having the output branches of the second and the third differential amplifier stage are formed with transistor whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at different values of the common control signals in the individual controllable amplifier arrangements (See Col. 5 line 66 to Col. 6 line 8).

Tiller et al. and Ishihara et al. are analogous, because both related to differential amplifier circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output

branches taught by Ihsihara et al.'s amplifier to applying to the amplifier of Tiller et al. for the purpose of providing gain control in differential circuit (Col. 4 line 11).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

November 3, 2003.

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
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